REMARKS

This communication responds to the Office Action mailed on March 17, 2005. Claim 1 is amended to provide proper antecedent basis, and not for reasons related to patentability. No claims are canceled, and no claims are added. As a result, claims 1-26 are now pending in this Application.

§101 Rejection of the Claims

Claims 24-26 were rejected under 35 USC § 101 because it is alleged that the claimed invention is directed to non-statutory subject matter. The Office Action states that "[c]laim 24 claims a recording medium on which a program is stored and variations thereof. These claims are therefore interpreted as recording a program per se ... language, specifically stating [sic] the claim, **must be** limited to a computer program stored on a computer recordable medium executing on a computer." [emphasis in original] The Applicants respectfully disagree. As noted by the court in *Alappat*:

> "Alappat admits that claim 15 would read on a general purpose computer programmed to carry out the claimed invention, but argues that this alone also does not justify holding claim 15 unpatentable as directed to nonstatutory subject matter. We agree. We have held that such programming creates a new machine, because a general purpose computer in effect becomes a special purpose computer once it is programmed to perform particular functions pursuant to instructions from program software. . . . The Supreme Court has never held that a programmed computer may never be entitled to patent protection. . . . Consequently, a computer operating pursuant to software may represent patentable subject matter, provided, of course, that the claimed subject matter meets all of the other requirements of Title 35." *In re Alappat*, 31 USPQ 2d 1545, 1558 (Fed. Cir. 1994) (en banc)

Claims 24-26 recite the structure of "[a]n article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing ...". These claims are therefore directed to an article of manufacture, including a system 500 executing code stored in a system memory 540 (see page 14 of the Application, lines 15-16), and as such, constitute patentable subject matter. The Applicants therefore respectfully request that the rejection under 35 USC § 101 be reconsidered and withdrawn.

§102 Rejection of the Claims

Claims 1-16 and 24-26 were rejected under 35 USC § 102(b) as being anticipated by Bowers (U.S. Patent No. 6,308,285; hereinafter "Bowers"). Claims 18 and 19 were rejected under 35 USC § 102(e) as being anticipated by Falik et al. (U.S. 6,065,078; hereinafter "Falik"). First, the Applicants do not admit that Bowers or Falik are prior art, and reserve the right to swear behind these references in the future. Second, since neither Bowers nor Falik anticipate each and every element of the invention as claimed by the Applicants, these rejections under 35 U.S.C. § 102 are respectfully traversed.

As admitted in the Office action, the sleep signal SLP# of Bowers is "delivered to *each* processor" such that "all processors are placed into a sleep mode." *See* Office Action, pg. 4, lines 6-8 and Bowers, Col. 2, line 53. This method of operation by Bowers is further supported by the Office Action admission that "The processors also stop executing commands ...". Office Action, pg. 4, line 10. That is, Bowers uses a controller (programmable array logic) to put each and every processor in the system to sleep, which is necessary, because this operation permits any one of the processors in Bowers to be physically replaced. *See* Bowers, Col. 2, lines 53-56. As a matter of contrast, in the embodiments claimed by the Applicants, one processor taken from the plurality of processors (e.g., the monarch processor) remains awake while other processors are put to sleep.

Given the method of operation disclosed in Bowers, the Office Action rejects the instant claims by attempting to characterize Bowers' controller as a "monarch processor." However, this is inappropriate. First, because Bowers makes a clear distinction between the "controller" and the "processors." It is *only* the controller in Bowers, and not the processors, that can access data used to put the processors to sleep. Second, even if one accepts the premise that Bowers' controller can operate as a monarch processor, the conclusion would be that Bowers' controller, as one of the plurality of processors, could also be put to sleep for replacement as directed by one of the other processors in Bowers' system. This type of operation, claimed by the Applicants, is not possible using Bowers' system.

Therefore, Bowers does not teach or suggest "a plurality of processors included in the computer system, wherein each processor of the plurality is capable of accessing the error handling routine on detecting an error and signaling remaining processors of the plurality of

processors to enter a rendezvous state" as claimed by the Applicants in independent claim 1 (and dependent claims 2-4). Bowers also does not teach or suggest a "monarch processor being capable of executing the error handling routine to correct the error ..." as claimed by the Applicants in independent claim 5 (and dependent claims 6-7) such that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state" as claimed in claim 7.

Further, Bowers does not teach or suggest "a plurality of processors including a monarch processor ... and an interrupt signaling mechanism ... to initiate a rendezvous state ... being a state where all of the plurality of processors but the monarch processor are idle" as claimed by the Applicants in independent claim 8 (and dependent claims 9-11). In addition, Bowers does not teach or suggest "a plurality of processors ... and an operating system layer ... to signal all but one of the plurality of processors to end a rendezvous state ... upon receiving a signal that error handling is completed, said rendezvous state being a state wherein all but the one of said plurality of processors are idle" as claimed by the Applicants in independent claim 12 (and dependent claims 13-15).

Bowers also does not teach or suggest "detecting an error ...; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; ... and ... correcting the error using the one processor" as claimed by the Applicants in independent claim 15 (and dependent claims 16-17). Finally, Bowers does not teach or suggest "attempting to correct an error ... in a multiple processor system ... and on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed by the Applicants in claim 24 (and dependent claims 25-26).

Falik suffers from similar deficiencies. Specifically, Falik fails to disclose "attempting to correct an error by a detecting processor included in a multiple processor system" and "entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed in claims 18 and 19. While the Office Action asserts that Falik's debugger interface is somehow equivalent to a "detecting processor included in a multiple processor system", this does not comport with the clear distinction Falik makes between the host computer 1820 and the multiprocessor integrated

circuit 1810. *See* Falik, Col. 2, lines 37-40 and FIG. 18. Even if it is assumed that Falik's debugger can operate as a "detecting processor", how does Falik's system correct the error? Falik's debugger, or a monitor, are the only resources available, and neither one operates to "correct" the error. It is respectfully noted that the term "error" appears only once in Falik, concerning bus communication error probability. However, such errors are not processed by Falik's system. *See* Falik, Col. 18, lines 31-32. In fact, Falik states that, while such errors can be cured by a system reset, such operation should be "avoided by the host" since this resets the entire chip. *See* Falik, Col. 18, lines 39-47.

Finally, how can "all but one of the processors included in the multiple processor system" be idle, as asserted in the Office Action, if at least one processor in the multiprocessor integrated circuit 1810 must be awake to execute a monitor, *in addition* to the debugger of Falik's host computer? The debugger communicates with the monitor on one of the processors, which means at least *two* processors must be operational in Falik's system. See Falik, Col. 17, lines 27-46.

In short, what is disclosed by Bowers and Falik is not identical to what is claimed by the Applicants, and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 1-16, 18-19, and 24-26 is respectfully requested.

§103 Rejection of the Claims

Claim 17 was rejected under 35 USC § 103(a) as being unpatentable over Bowers, in view of Fujii et al. (U.S. 5,892,898; hereinafter "Fujii"). First, the Applicants do not admit that Bowers or Fujii are prior art, and reserve the right to swear behind these references in the future. Second, because a *prima facie* case of obviousness has not been established, the Applicants respectfully traverse this rejection under 35 U.S.C.§103(a).

First, there is no motivation to combine Bowers and Fujii. Bowers never uses the term "error", or discloses any type of error detection or handling routine. Processor boards are simply replaced after the fact – notably, for routine maintenance. *See* Bowers, Col. 4, lines 29-34 Similarly, Fujii never mentions removing a processor from a system.

Second, the Office mischaracterizes the claimed "severe error" (which causes entry into a rendezvous state) as a "non-recoverable problem" documented by Fujii? However, this

characterization does not comport with the concept of a "rendezvous state" claimed by the Applicants:

> "An example of this type of error is a parity error in the processor instruction cache. In this case, firmware will invalidate the entire instruction cache, access another copy of the instruction, and resume execution of the interrupted process. This type of error can be signaled to a processor by the platform via a double bit ECC error on the system bus. This type of error is generally corrected by entering the rendezvous state." Application, pg. 7, lines 19-24.

Thus, contrary to the assertion in the Office Action, it would not have been obvious to "make the modification because an error event type is used to report a non-recoverable problem ... and a warning event type is used to indicate some kind of recoverable anomaly ... [k]nowing the severity of the event determines what action should be taken (removal of a processor)." Office Action, pg. 15, lines 14-17. That is, the instant invention contemplates a recoverable error as a reason to enter the rendezvous state, not a non-recoverable one.

Third, it is not necessarily true that "knowing the severity of the event determines what action should be taken (e.g., removal of a processor)" as asserted in the Office Action. Errors of varying severity can occur within a computer system, and knowledge of the severity (e.g., non-recoverable) will not always be determinative as to whether a processor should be replaced (e.g. a main memory failure may be the culprit, or a hard disk failure, etc.). Since there is no evidence in the record to support the Office Action assertion, the explicit requirements set forth by *In re Sang Su Lee* are not satisfied. Therefore, the Examiner appears to be using personal knowledge, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Fourth, it should be noted that neither Bowers nor Fujii disclose using a processor that is part of a multi-processor system to correct an error within the system, as claimed by the Applicants (i.e., "detecting an error by one processor included in a multiple processor system; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; [and] correcting the error using the one processor" in claim 15, from which 17 depends). Thus, no combination of Bowers and Fujii can provide this element.

Fifth, combining Bowers with Fujii gives no reasonable expectation of success. Fujii merely teaches the existence of an error recording system, not a system to correct errors. The mechanism of replacing a processor (as taught by Bowers) in response to recording non-

recoverable errors, advocated in the Office Action, also may not have any effect on solving the actual problem (e.g., a main memory failure, or a cache failure).

Since there is no motivation to combine the references, since no combination of the references can be made which teaches the claimed invention, and since combination gives no reasonable expectation of success, no *prima facie* case of obviousness has been established, and the Applicants respectfully request reconsideration and withdrawal of the rejection with respect to claim 17 under 35 U.S.C. §103.

Allowable Subject Matter

The Applicants note with appreciation that claims 21-23 have been allowed. Claim 20 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, since it is believed that claims 18-19 are in condition for allowance, the Applicants respectfully decline to amend claim 20 to include the limitations of claims 18-19.

Conclusion

The Applicants respectfully submit that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney, Mark Muller at (210) 308-5677, or Applicant's below-named representative to facilitate the prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SURESH MARISETTY ET AL.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of May 2005.

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Signature